B1

1. (Once Amended) A method for forming gate electrodes of a semiconductor device, the method comprising:

forming a gate insulation layer over a semiconductor wafer;

forming a conductive layer over the gate insulation layer;

forming a low-dielectric layer over the conductive layer;

forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

removing the photoresist pattern and shrinking the low-dielectric pattern, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time; and

forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

B2

3. (Once Amended) The method of claim 1, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the conductive layer for the gate electrodes; and

soft-baking the low-dielectric layer at a predetermined temperature.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

--11. (New) A method for forming gate electrodes of a semiconductor device, the method comprising:

forming a gate insulation layer over a semiconductor wafer;

forming a conductive layer over the gate insulation layer;

forming a low-dielectric layer over the conductive layer;

soft-baking the low-dielectric layer at a predetermined temperature;

forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

removing the photoresist pattern;

shrinking the low-dielectric pattern after the removal of the photoresist pattern; and

forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

B3

12. (New) The method of claim 11, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the conductive layer for the gate electrodes.

13. (New) The method of claim 11, wherein shrinking the low-dielectric pattern includes curing the low-dielectric pattern at a temperature of 400-500°C.--

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com